UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/758,040 | 01/16/2004 | Sung-kyu Choi | Q78894 | 6125 |

23373 7590 01/11/2008

SUGHRUE MION, PLLC
2100 PENNSYLVANIA AVENUE, N.W.
SUITE 800
WASHINGTON, DC 20037

| EXAMINER | |
|---|---|
| LEE, CHRISTOPHER E | |
| **ART UNIT** | **PAPER NUMBER** |
| 2111 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 01/11/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

**BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES**

**MAILED**

**JAN 11 2008**

**Technology Center 2100**

Application Number: 10/758,040
Filing Date: January 16, 2004
Appellant(s): CHOI, SUNG-KYU

Mark E. Wallerson (Reg. No. 59,043)
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed on 2nd of November 2007 appealing from the Office action mailed on 18th of January 2007.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

| | | |
|---|---|---|
| US 5,509,124 A | Bourke et al. | 04-1996 |
| US 2003/0084226 A1 | Barrenscheen et al. | 05-2003 |
| JP 2000-92365 A | Masayuki et al. | 03-2000 |
| US 5,239,651 A | Sodos, Martin | 08-1993 |
| US 6,265,885 B1 | Luo et al. | 07-2001 |

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bourke et al. [US 5,509,124 A; hereinafter Bourke] in view of Barrenscheen et al. [US 2003/0084226 A1; Barrenscheen]

*Referring to claim 1,* Bourke discloses a buffering apparatus (i.e., IOIC 10j-m in Fig. 2, standing for Input Output Interface Controller) comprising:

- an asynchronous data bus write unit (i.e., means for processing storage read command in storage operation control 40b2 in Fig. 16) which, when control information (i.e., during control signal ACTIVATE READY being **not asserted**) indicating a request for writing in a buffer (i.e., loading data into registers and buffers 20 of Fig. 2) connected to an asynchronous data bus (i.e., SPD bus 10t-w in Fig. 2) not synchronized with a processor (i.e., instruction processor unit 10a of Fig. 1) is provided by a multiplexer (i.e., adapter interface 14 of Fig. 2A with adapter bus control logic 30 of Fig. 2) connected to the processor (i.e., said instruction processor unit; See col. 17, lines 59-64), receives third data (i.e., data being read from common memory facility 10d in Fig. 1) from the multiplexer (i.e., said adapter interface with adapter bus control logic, in fact said adapter bus delivering said data), stores the third data (i.e., loading said data into said registers and buffers; See col. 17, lines 59-61), and transfers the stored third data to a second memory (i.e., IOBU 10p-s in Fig. 1, standing for Input Output Bus Unit, e.g., serial presence detect (SPD) EEPROM) through the asynchronous data bus (i.e., said SPD bus; See col. 17, lines 61-64); and

- an asynchronous data bus read unit (i.e., means for processing storage write command in storage operation control 40b2 in Fig. 16) which, when control information (i.e., control signal DATA IN END being **asserted**) indicating a request for reading from the buffer (i.e., unloading data from said registers and buffers) is provided by the multiplexer (i.e., said adapter interface with adapter bus control logic; See col. 17, lines 50-59), receives fourth data (i.e., data to be written to said common memory facility) from the second memory (i.e., said IOBU, e.g., SPD EEPROM) through the asynchronous data bus (i.e., said SPD bus; See col. 17, lines 50-54), stores the fourth data (i.e., loading said data to be written to said common memory facility into said registers and buffers; See col. 17, line 55), and transfers the stored fourth data to the multiplexer (i.e., said adapter interface with adapter bus control logic; See col. 17, lines 55-59).

Bourke does not teach that the multiplexer receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor.

Barrenscheen discloses a data transmission device (i.e., data transmission unit in Fig. 1; See Abstract, paragraph [0001]), wherein

- a multiplexer (i.e., Bus Interface BI1 in Fig. 4) receives first data from a processor (e.g., Module BU11 in Figs. 2A-B; See paragraph [0029]) and transfers the received first data to a first memory (e.g., Module BU12 in Figs. 2A-B; See paragraph [0029]) through a synchronous data bus (i.e., BUS1 in Figs. 2A-B) synchronized with the processor (See paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A), or receives second data from the first memory through the synchronous data bus and transfers the received second data to

the processor (See paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data transmission device (i.e., data transmission unit), as disclosed by Barrenscheen, in said buffering apparatus (i.e., Input Output Interface Controller), as disclosed by Bourke, for the advantage of providing a way of transmitting large volumes of data quickly and efficiently with a low level of involvement (See Barrenscheen, paragraph [0011]).

Claims 2-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki et al. [JP 2000-92365 A; cited by the Applicant; hereinafter Masayuki] in view of Barrenscheen [US 2003/0084226 A1]

*Referring to claim 2,* Masayuki discloses a processor bus connection method (i.e., a method for preventing congestion in an image data bus to allow each circuit to efficiently conduct signal processing; See Abstract) comprising:

- (a)' when address information indicating an address of a first memory (i.e., address of recording apparatus 51 of Fig. 2) connected to a synchronous data bus (i.e., CPU bus 34 of Fig. 2) synchronized with a processor (i.e., CPU 41 of Fig. 2), from the processor is received (i.e., addressing command being executed by said CPU), transferring first data (i.e., compressed image data) to the first memory through the synchronous data bus (See paragraph [0029]); and
- (b)' when address information indicating an address of a second memory (i.e., address of image memory 32 of Fig. 2) connected to an asynchronous data bus not synchronized with the processor (i.e., image data bus 33 of Fig. 2), from the processor is received (i.e.,

addressing command being executed by said CPU), transferring third data (i.e., image data from input device, e.g., CCD image sensor 11 of Fig. 2) to the second memory through the asynchronous data bus (See paragraph [0028]).

Masayuki does not teach (a) when address information indicating the address of the first memory connected to the synchronous data bus, from the processor is received, receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus, or receiving second data from the first memory through the synchronous data bus and transferring the received second data to the processor; and (b) when address information indicating the address of the second memory connected to the asynchronous data bus, from the processor is received, receiving the third data from the processor, transferring the third data, storing the transferred third data, and transferring the stored third data to the second memory through the asynchronous data bus, or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor.

Barrenscheen discloses a method for data transmission forwarding data (See Abstract and paragraph [0001]) comprising:

- (a) when address information indicating an address of a first memory (i.e., address of Module BU12 in Figs. 2A-B) connected to a synchronous data bus (i.e., BUS1 in Figs. 2A-B) synchronized with a processor (i.e., Module BU11 in Figs. 2A-B), from the processor is received (See paragraph [0035], lines 1-4; actually, data transmission between devices connected to said BUS1 in Fig. 2A), receiving first data from the processor and transferring the received first data to the first memory through the synchronous data bus (See paragraph [0035], lines 11-12; for example, DMA data

writing operation from said Module BU11 to said Module BU12 in Fig. 2A), or receiving second data from the first memory through the synchronous data bus and transferring the received second data to the processor (See paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A); and

- (b) when address information indicating an address of a second memory (i.e., address of Module BU23 in Figs. 2A-B) connected to an asynchronous data bus (i.e., BUS2 in Figs. 2A-B) not synchronized with the processor (i.e., said Module BU11, which is synchronized with said BUS1, not said BUS2), from the processor is received, receiving third data from the processor, transferring the third data, storing the transferred third data (i.e., data stored in IM Buffer Store in Fig. 4), and transferring the stored third data to the second memory (i.e., said Module BU23) through the asynchronous data bus (See paragraph [0036]; for example, data writing operation from said Module BU11 to said Module BU23 via bus bridge in Fig. 2B), or receiving fourth data from the second memory through the asynchronous data bus, storing the fourth data, transferring the stored fourth data, receiving the transferred fourth data, and transferring the received fourth data to the processor (See paragraph [0036]; for example, data reading operation from said Module BU23 to said Module BU11 via bus bridge in Fig. 2B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method for data transmission forwarding data, as disclosed by Barrenscheen, in said processor bus connection method (i.e., a method for preventing congestion in an image data bus to allow each circuit to efficiently conduct signal processing), as disclosed by Masayuki, for the advantage of providing a way of transmitting large volumes of

data quickly and efficiently with a low level of involvement (See Barrenscheen, paragraph [0011]).

*Referring to claim 3,* Barrenscheen teaches (a) comprising

- (a1) when the address information indicating the address of the first memory (i.e., address of Module BU12 in Figs. 2A-B) is provided by the processor (i.e., Module BU11 in Figs. 2A-B) and a control information indicating a request for writing in the first memory is provided by the processor (i.e., DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A), receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus (See paragraph [0035], lines 1-4 and 11-12; i.e., wherein in fact that the data transmission device DTU as a DMA controller in fact transfers data from the device BU11 to the device BU12 clearly anticipates that a control information indicating a request for writing in the first memory is provided by the processor, receiving the first data from the processor and transferring the received first data to the first memory through the synchronous data bus); and
- (a2) when the address information indicating the address of the first memory (i.e., address of said Module BU12) is provided by the processor (i.e., said Module BU11) and the control information indicating the request for reading from the first memory is provided by the processor (i.e., DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A), receiving the second data from the first memory through the synchronous data bus and transferring the received data to the processor (See paragraph [0035], lines 1-4 and 11-12; i.e., wherein in fact that the data transmission device DTU as a DMA controller can transmit data from one of the devices connected to

the bus BUS1 to another of the devices connected to the BUS 1, and said DTU in fact transfers data from the device BU11 to the device BU12, as an example shown in Fig. 2A, clearly anticipates that the control information indicating the request for reading in the first memory is provided by the processor, receiving the second data from the processor and transferring the received data to the processor).

*Referring to claim 4,* Masayuki discloses a synchronous bus (i.e., CPU bus 34 of Fig. 2) and asynchronous bus (i.e., image data bus 33 of Fig. 2) path method (in fact, a method for preventing congestion in an image data bus to allow each circuit to efficiently conduct signal processing; See Abstract) comprising:

- (a) receiving input data (i.e., receiving image data from CCD image sensor 11 in Fig. 2) and transferring the received input data (i.e., said image data) through an asynchronous data bus (i.e., image data bus 33 of Fig. 2) not synchronized with a processor (i.e., CPU 41 of Fig. 2), then transferring the input data (i.e., compressed image data after said image data being processed by JPEG encoder/decoder 29 in Fig. 2) through a synchronous data bus (i.e., CPU bus 34 of Fig. 2) synchronized with the processor (i.e., said CPU); and
- (b) receiving the input data (i.e., said compressed image data) through the synchronous bus and transferring the received input data (See paragraph [0029]).

Masayuki does not teach (c) generating first data or third data from the transferred input data and transferring the generated first or third data; (d) receiving the first data, transferring the received first data to a first memory through the synchronous data bus, or receiving and storing the third data and transferring the stored third data to a second memory through an asynchronous bus not synchronized with the processor; (e) receiving the first data through

the synchronous bus and storing the data; and (f) receiving the third data through the asynchronous bus and storing the data.

Barrenscheen discloses a synchronous bus and asynchronous bus path method (i.e., a method for data transmission forwarding data on a first and second data busses; See Abstract and paragraph [0001]), wherein a data transmission unit (i.e., DTU in Figs. 2A-B) performs the step of

- (c) generating first data (i.e., data from DTU toward Module BU12 on BUS1 in Fig. 2A) or third data (i.e., data from DTU toward Module BU23 on BUS2 in Fig. 2B) from transferred input data and transferring the generated first or third data (See paragraphs [0034]-[0036]);
- (d) receiving the first data, transferring the received first data to a first memory (i.e., Module BU12 in Figs. 2A-B) through the synchronous data bus (See Fig. 2A and paragraph [0035], lines 11-12), or receiving and storing the third data (i.e., data stored in IM Buffer Store in Fig. 4) and transferring the stored third data to a second memory (i.e., Module BU23 in Figs. 2A-B) through an asynchronous bus (i.e., BUS2 in Figs. 2A-B; See paragraph [0036]) not synchronized with the processor (i.e., said Module BU11, which is synchronized with said BUS1, not said BUS2);
- (e) receiving the first data through the synchronous bus and storing the first data (See paragraph [0035] and Fig. 2A, wherein data are transferred via DMA controlling, i.e., received and stored through said BUS1 by DMA transferring operation); and
- (f) receiving the third data through the asynchronous bus and storing the third data (See paragraph [0036] and Fig. 2B, wherein data are transferred via bus bridging, i.e., received and stored via said BUS2 by bus bridge transferring operation).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said data transmission unit (i.e., DTU), as disclosed by Barrenscheen, in said path between said synchronous bus (i.e., CPU bus) and said asynchronous bus (i.e., image data bus), as disclosed by Masayuki, for the advantage of providing a way of transmitting large volumes of data quickly and efficiently with a low level of involvement (See Barrenscheen, paragraph [0011]).

*Referring to claim 5,* Masayuki, as modified by Barrenscheen, teaches

- (g) transferring second data through the synchronous bus (i.e., data transferring through BUS1 in Fig. 2A; See Barrenscheen, paragraph [0035], lines 11-12);
- (h) transferring fourth data through the asynchronous bus (i.e., data transferring through BUS2 in Fig. 2B; See Barrenscheen, paragraph [0036]);
- (i) receiving the second data through the synchronous bus and transferring the received second data (See Barrenscheen, paragraph [0035]), or receiving the fourth data through the asynchronous bus, storing the fourth data (i.e., data being stored in IM Buffer Store in Fig. 4; Barrenscheen), and transferring the stored fourth data (See Barrenscheen, paragraphs [0036] and [0043]);
- (j) generating output data (i.e., OSD image memory 32 generates character image in Fig. 2; Masayuki) from the second data or fourth data (See Masayuki, paragraph [0024]) and transferring the output data (i.e., transferring said generated character image to said memory controller in Fig. 1; Masayuki);
- (k) receiving and storing the output data (i.e., bit map data are stored in said memory controller for controlling) and transferring the stored output data through the

asynchronous bus (i.e., transferring said OSD and image data to NTSC/PAL encoder 23 via image data bus 33 for composition in Fig. 2; See Masayuki, paragraph [0024]); and

- (l) receiving the output data through the asynchronous bus (See Masayuki, paragraph [0024]) and outputting the received output data (See Masayuki, paragraphs [0031]-[0033]).

*Referring to claim 6,* Masayuki teaches

- if the received output data or the received third data is display data (i.e., OSD and/or image data; See paragraph [0024]), the received output data is displayed (i.e., displayed on finder 36 in Fig. 2).

Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki [JP 2000-92365 A] in view of Barrenscheen [US 2003/0084226 A1] as applied to claims 2-6 above, and further in view of Sodos [US 5,239,651 A]

*Referring to claim 7,* Masayuki, as modified by Barrenscheen, discloses all the limitations of the claim 7, except that does not expressly teach giving permission on the use of the synchronous bus; and giving permission on the use of the asynchronous bus.

Sodos discloses a method of arbitration for multiple requested data transfers (See Abstract), wherein

- (m) giving permission (i.e., bus grant) on the use of a synchronous bus (e.g., Internal Busses 240 of Fig. 2); and
- (n) giving permission (i.e., bus grant) on the use of an asynchronous bus (e.g., External Busses 230 of Fig. 2; See col. 5, lines 3-33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of arbitration for multiple requested data transfers, as disclosed by Sodos, in said method for said synchronous and asynchronous busses path, as disclosed by Masayuki, as modified by Barrenscheen, for the advantage of providing an efficient resource utilization for a resource handling multiple time multiplexing data transfer operations (See Sodos, col. 2, lines 26-32).

*Referring to claim 8,* Masayuki, as modified by Barrenscheen and Sodos, teaches

- in (a) and (b), the received input data is transferred through the synchronous bus and the input data is received through the synchronous bus (i.e., data being transferred through BUS1 in Figs. 2A-B; Barrenscheen) for which permission to use is given in (m) (i.e., said BUS1 is granted to transfer said data; See Sodos, col. 5, lines 3-33);
- in (d), the received first data is transferred to the first memory (i.e., data being transferred to Module BU12 in Figs. 2A-B; Barrenscheen) through the synchronous data bus and the first data is received through the synchronous bus and stored (i.e., transferred to said Module BU12; See Barrenscheen, Fig. 2A and paragraph [0035], lines 11-12) for which permission to use is given in (m) (i.e., said Module BU12 is granted to transfer said data; See Sodos, col. 5, lines 3-33), or the stored third data (i.e., data stored in IM Buffer Store in Fig. 4; Barrenscheen) is transferred to a second memory (i.e., data being transferred to Module BU23 in Figs. 2A-B; Barrenscheen) through the asynchronous bus (i.e., BUS2 in Figs. 2A-B; See Barrenscheen, paragraph [0036]) for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33);

- in (f), the third data is received through the asynchronous bus (i.e., BUS2 in Figs. 2A-B; See Barrenscheen, paragraph [0036] and Fig. 2B) for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33) and stored (in fact, data are transferred via bus bridging, i.e., received and stored via said BUS2 by bus bridge transferring operation; Barrenscheen).

*Referring to claim 9,* Masayuki, as modified by Barrenscheen and Sodos, teaches

- in (g), the second data is transferred through the synchronous bus (i.e., data transferring through BUS1 in Fig. 2A; See Barrenscheen, paragraph [0035], lines 11-12) for which permission to use is given in (m) (i.e., said BUS1 is granted to transfer said data; See Sodos, col. 5, lines 3-33);
- in (h), the fourth data is transferred through the asynchronous bus (i.e., data transferring through BUS2 in Fig. 2B; See Barrenscheen, paragraph [0036]) for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33);
- in (i), the second data is received through the synchronous bus (i.e., said BUS1) for which permission to use is given in (m) (i.e., said BUS1 is granted to transfer said data; See Sodos, col. 5, lines 3-33) and the received second data is transferred (See Barrenscheen, paragraph [0035]), or the fourth data is received through the asynchronous bus for which permission to use is given in (n) (i.e., said BUS2 is granted to transfer said data; See Sodos, col. 5, lines 3-33), stored (i.e., data being stored in IM Buffer Store in Fig. 4; Barrenscheen), and the stored fourth data is transferred (See Barrenscheen, paragraphs [0036] and [0043]);

- in (k) the output data (i.e., bit map data are stored in said memory controller for controlling; Masayuki) is received and stored, and the stored output data is transferred through the asynchronous bus (i.e., transferring said OSD and image data to NTSC/PAL encoder 23 via image data bus 33 for composition in Fig. 2; See Masayuki, paragraph [0024]) for which permission to use is given in (n) (i.e., said image data bus is granted to transfer said data; See Sodos, col. 5, lines 3-33); and
- in (l), the output data is received through the asynchronous bus (See Masayuki, paragraph [0024]) and the received output data is output to a user (i.e., user of digital still camera in Fig. 2; See Masayuki, paragraphs [0031]-[0033]) for which permission to use is given in (n) (i.e., said image data bus is granted to transfer said data; See Sodos, col. 5, lines 3-33) and the received third data is output (i.e., displaying on finder 36 of Fig. 2; Masayuki).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masayuki [JP 2000-92365 A] in view of Barrenscheen [US 2003/0084226 A1] and what was well known in the art, as exemplified by Luo et al. [US 6,265,885 B1; hereinafter Luo]

*Referring to claim 10,* all of the claim limitations have already been discussed/addressed with respect to claim 4, with the exception of a tangible computer readable recording medium including a computer program having instructions for controlling a synchronous bus and asynchronous bus, the instructions comprising the steps of the method in the claim 4 (e.g., implementing in a computer software program).

The Examiner takes Official Notice that said method in the claim 4 being implemented in a computer program having instructions for controlling said synchronous bus and asynchronous bus (i.e., a computer software program), and being stored in a tangible computer readable

recording medium (e.g., ROM; See Application, page 49, line 1), is well known to one of ordinary skill in the art, as evidenced by Luo (See Claim 9, lines 2-4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have implemented said method of the claim 4 in said computer program having said instructions (i.e., a computer software program), and being stored in said tangible computer readable recording medium (i.e., read-only memory; See Luo, col. 3, lines 38-54) since it would have provided a better flexibility of implementing said method than a hardware implementation, such as an easy modification, etc.

Furthermore, the recitation in the claim 10, that "a tangible computer readable recording medium including a computer program" has not been given patentable weight because it has been held that a preamble is denied the effect of a limitation where the claim is drawn to a structure and the portion of the claim following the preamble is a self-contained description of the structure not depending for completeness upon the introductory clause. *See Kropa v. Robie, 88 USPQ 478 (CCPA 1951).*

**(10) Response to Argument**

*In response to the Appellant's argument with respect to* "Claim 1 recites in part: wherein the multiplexer receives first data from the processor and transfers ... The Examiner asserts that Barrenscheen discloses this feature of the claim and apparently reads the claimed multiplexer on Bus Interface (BI1) as disclosed by Barrenscheen. Appellant respectfully submits that the Bus Interface BI1 is not a multiplexer. Instead, Bus Interfaces BI1-BI4 are used to connect the data transmission device DTU to the first through fourth buses BUS1-BUS4, respectively. Consequently, Bus Interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen. ... Appellant respectfully submits that claim 1 would not have been rendered obvious by Bourke and Barrenscheen. There is simply no disclosure of, nor has the Examiner provided specific support in Barrenscheen that the Bus interface, BI1 acts as or performs the functions of a multiplexer." in the Appeal Brief page 10, line 7 through page 11, line 7, the Examiner respectfully disagrees.

In fact, the Appellant recites the claimed subject matter "multiplexer" in the limitation "wherein **the multiplexer** receives first data from the processor and transfers the received first data to a first memory through a synchronous data bus synchronized with the processor, or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor" (See Claim 1, lines 11-14).

Therefore, in contrary to the Appellant's assertion, i.e., bus interface BI1 does not perform the functions of and is not described as a multiplexer in Barrenscheen, Barrenscheen is clearly suggesting that the claimed subject matter "**multiplexer**" (i.e., being equalized to **Bus Interface BI1** in Fig. 4) receives first data from a processor (e.g., Module BU11 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) and transfers the received first data to a first memory (e.g., Module BU12 in Figs. 2A-B; See Barrenscheen, paragraph [0029]) through a synchronous data

bus (i.e., BUS1 in Figs. 2A-B) synchronized with the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data writing operation from said Module BU11 to said Module BU12 in Fig. 2A, wherein said Module BU11 should be synchronized with said BUS1 for said DMA data writing operation), or receives second data from the first memory through the synchronous data bus and transfers the received second data to the processor (See Barrenscheen, paragraph [0035], lines 11-12; for example, DMA data reading operation from said Module BU12 to said Module BU11 in Fig. 2A, wherein said Module BU12 should be synchronized with said BUS1 for said DMA data reading operation). In other words, the recited claiming language "multiplexer," and its function in the exemplary claim 1 are interpreted as the bus interface BI1 performs the same functions of and is described as the claimed subject matter "multiplexer" in Barrenscheen.

Furthermore, the Applicant defines that the claimed subject matter "multiplexer" is no more specific component than an interfacing component among processor, buffer, synchronous data bus, and asynchronous data bus, in the specification, page 20, paragraphs [54]-[55], and Figs. 3-4. Even though the language "multiplexer" is defined as "being or relating to a system of transmitting several messages or signals simultaneously on the same circuit or channel" in Merriam-Webster's Collegiate® Dictionary (10th ed.), the Applicant defines the claimed subject matter "multiplexer" as an interfacing component among processor, buffer, synchronous data bus, and asynchronous data bus, in the specification, as is shown herein *Supra*.

Therefore, Barrenscheen discloses the subject matter "Bus interface BI1," which is acting as or performing the functions of the claimed subject matter "multiplexer" within the scope of the claimed invention.

Thus, Appellant's argument for this point cannot be seen as persuasive.

*In response to the Appellant's argument with respect to* "The Examiner also maintains that Barrenscheen discloses that BUS1 in FIGS. 2A-B is synchronized with the processor, and cites paragraph [0035] of Barrenscheen as allegedly disclosing this feature of claim 1. However, paragraph [0035] merely discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the same bus or between devices connected between different buses autonomously. Although the DTU which is used as a DMA in Barrenscheen may transfer data between BUS1 and BUS2 and between their respective devices, Barrenscheen does not require BUS1 and BUS2 be synchronized with the processor. Appellant respectfully submits that there is simply no disclosure in Barrenscheen that the BUS1 is synchronized with a processor." in the Appeal Brief page 11, lines 8-16, the Examiner respectfully disagrees.

As the Appellant admitted, Barrenscheen discloses that when the data transmission device (DTU) is used as a DMA controller, it can transmit data between devices connected to the same bus or between devices connected between different buses autonomously, in the paragraph [0035]. This disclosure in Barrenscheen inherently anticipates that the Modules BU11 or BU21 as a processor sends DMA (Direct Memory Access) command for the DMA operation (e.g., data bursting) to the DTU via the bus BUS1 or BUS2 in Fig. 3, which is clearly teaching said busses BUS1 and BUS2 should be synchronized with said Modules BU11 and BU21 because said Modules BU11 and BU21 should be able to communicate with said DTU for said DMA operation being performed among synchronized components, e.g., DMA device, Bus, Chipset, Memory, etc.

If the Appellant's argument is correct, *arguendo*, the Examiner as one of the ordinary skill in the art doubts how the invention of Barrenscheen supports said DMA operation without requiring said BUS1 and BUS2 be synchronized with the processor.

Furthermore, the Appellant fails to provide any supporting evidence why Barrenscheen does not require BUS1 and BUS2 be synchronized with the processor except the mere allegation. Therefore, in contrary to the Appellant's allegation, Barrenscheen inherently anticipates the claimed subject matter "a synchronous data bus synchronized with the processor" in the representative claim 1, such that the busses BUS1 and BUS2 should be synchronized with said Modules BU11 and BU21 because the Modules BU11 or BU21 as a processor sends DMA command for the DMA operation to the DTU via the bus BUS1 or BUS2 in Fig. 3.
Thus, Appellant's argument for this point cannot be seen as persuasive.

*In response to the Appellant's argument with respect to* "With respect to independent claims 2, 4, and 10, the Examiner asserts that Masayuki teaches both a synchronous bus and an asynchronous bus as required by independent claims 2, 4, and 10 and cites bus 34 and bus 33 of Masayuki as allegedly respectively reading on the claimed synchronous and asynchronous buses. Appellant respectfully submits that it appears that the Examiner is merely assuming that CPU bus 34 is (synchronous) synchronized with CPU 41, and that image data bus 33 is (asynchronous) not synchronized with CPU 41 because image data bus 33 is not directly connected to CPU 41 in Fig. 2. However, nowhere does Masayuki disclose that image data bus 33 is asynchronous. Moreover, Masayuki does not disclose any terms related to 'synchronous' and 'asynchronous'." in the Appeal Brief page 12, lines 1-11, the Examiner respectfully disagrees.

Actually, the Examiner has shown that Masayuki teaches the claimed limitation "a synchronous data bus synchronized with a processor," such that CPU bus 34 is (synchronous) synchronized with CPU 41 in Fig. 2 (See Masayuki, paragraph [0029]). Furthermore, the Examiner has additionally shown that Masayuki teaches the claimed limitation "an

asynchronous data bus not synchronized with the processor," such that image data bus 33 is (asynchronous) not synchronized with CPU 41 in Fig. 2 (See Masayuki, paragraphs [0016]-[0017] and [0028]; wherein in fact that said image data bus is used for supplying image data from CCD image sensor 11 to image memory 32 or from said image memory 32 to view finder 36 in Fig. 2, which is not synchronized with said CPU 41, but synchronized with means for signal processing in order to prevent delay of said image data bus; See furthermore, Masayuki, paragraphs [0019]-[0020]).

However, in contrary to the Appellant's assertion, the Examiner has never stated during the prosecution that the image data bus 33 is not synchronized with CPU 41 because said image data bus is not directly connected to said CPU in Fig. 2. In fact, the connection status between said image data bus and said processor in the schematic drawing, Fig. 2, of Masayuki, cannot definitely state the operating status, i.e., synchronized or not synchronized with the processor, in detail. Instead, the Examiner stresses that the invention of Masayuki uses several interface logics, i.e., Memory Interface 27, Host Interface 31, and JPEG Interface 30 in Fig.1, between said image data bus and said CPU bus, which are not necessarily required in the Masayuki invention if said image data bus is synchronized with said CPU. In other words, said several interface logics are needed for interfacing between said image data bus and said CPU because said image data bus is not synchronized with said CPU, which is clearly teaching the claimed limitation "an asynchronous data bus not synchronized with the processor."

Furthermore, even though Masayuki does not use the terms related to "synchronous" and "asynchronous," it is clear that Masayuki inherently anticipates the argued elements, as is shown in the above.

Thus, Appellant's argument for this point cannot be seen as persuasive.

*In response to the Appellant's argument with respect to* "First, there is simply no teaching or suggestion in Masayuki of synchronous and asynchronous buses. ... Nowhere does Masayuki expressly disclose synchronizing a data bus with a processor. At best, Masayuki discloses that the sink generator 26 may provide a synchronization signal (for example a clock signal), not to the image bus 33, but only to the timing generator 13, wherein the timing generator 13 generates a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator (see the signal lines of FIG. 1 and paragraphs [0014] and [0017]). In other words, the synchronization signal generated by the sink generator 26 is only for generating a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator 10." in the Appeal Brief page 13, lines 1-12, the Examiner respectfully disagrees.

At first, if the Appellant's assertion is correct, *arguendo*, such that the CPU bus 34 (i.e., data bus) is not synchronized with the CPU 41 in Fig. 2 of Masayuki because Masayuki does not expressly disclose synchronizing said CPU bus with said CPU, the Examiner, as one of ordinary skill in the art, doubts how said CPU 41 could write image data in a recording device 51 through said CPU bus 34 in Fig. 2 (See paragraph [0029]). Therefore, even though Masayuki does not expressly states synchronizing said CPU bus with said CPU, it is inherently anticipated such that said CPU should be synchronized with said CPU bus for writing image data in said recording device through said CPU bus.

At second, the Examiner notices that the Appellant states the element SG 26 in Fig. 1 of Masayuki as "sink generator." However, it is not a **sink** generator, but a **sync** generator, which is generating video sync signals for image signals (See paragraphs [0016]-[0017]).
And, the Appellant argues that the sync generator may provide a synchronization signal, not to the image bus, but only to the timing generator 13 in Fig. 1, wherein the synchronization signal

generated by said sync generator is only for generating a horizontal synchronization signal and a vertical synchronization signal controlling every circuit of the image generator. However, this argument does not definitely confine that the image data bus is synchronized with the CPU, and thus, the Appellant cannot assert that Masayuki does not teach the claimed limitation "an asynchronous bus (i.e., image data bus) not synchronized with the processor (i.e., CPU)."
In fact, Masayuki uses several interface logics, i.e., Memory Interface 27, Host Interface 31, and JPEG Interface 30 in Fig.1, between said image data bus and said CPU bus, which are not necessarily required in the Masayuki invention if said image data bus is synchronized with said CPU. In other words, said several interface logics are needed for interfacing between said image data bus and said CPU because said image data bus is not synchronized with said CPU, which is clearly teaching the claimed limitation "an asynchronous data bus not synchronized with the processor."
Thus, Appellant's argument for this point cannot be seen as persuasive.

*In response to the Appellant's argument with respect to* "Appellant also respectfully submits that it appears that the image bus 33 is synchronized with CPU 41 as CPU bus 34, because the image bus 33 is directly connected to the CPU bus 34, not via a buffer, as illustrated in FIG. 2 of Masayuki. Therefore, the Examiner's assertion that image bus 33 is an asynchronous data bus not synchronized with the processor and synchronized with the sink generator is clearly erroneous." in the Appeal Brief page 13, lines 13-17, the Examiner respectfully disagrees.

As discussed in the above response, no one can definitely state that the image data bus 33 is synchronized with CPU 41 as CPU bus 34 with only the reason of direct line connection between said image data bus and said CPU bus, not via a buffer, in Fig. 2 because the

schematic diagram in Fig. 2 cannot show everything of the Masayuki invention in detail. Moreover, even though said buffer is not shown between said image data bus and said CPU bus in Fig. 2, another drawing Fig 1 clearly shows at least three interface logics, i.e., Memory Interface 27, Host Interface 31, and JPEG Interface 30, between said image data bus and said CPU bus. In other words, said at least three interface logics are needed for interfacing between said image data bus and said CPU because said image data bus is not synchronized with said CPU, which is clearly teaching the claimed limitation "an asynchronous data bus not synchronized with the processor."

Thus, Appellant's argument for this point cannot be seen as persuasive.

*In response to the Appellant's argument with respect to* " Further, the fact that Masayuki teaches a signal processing unit which prevents delay of image data does not necessarily mean that this 'inherently' teaches that the image data bus is synchronized with the CPU as alleged by the Examiner." in the Appeal Brief page 14, lines 1-3, the Examiner respectfully disagrees.

In contrary to the Applicant's statement, the Examiner has never alleged that the image data bus 35 is synchronized with the CPU 41 in Fig. 2. Instead, the Examiner pointed out said image data bus not being synchronized with said CPU because Masayuki inherently anticipates the claimed limitation "an asynchronous bus not synchronized with the processor," such that a memory controller 22 arbitrates said image data bus, and performs data transfer to CPU bus 34 in Fig. 1, which is clearly showing that said image data bus is not synchronized with CPU (See Masayuki, paragraph [0036]). If said image data bus is synchronized with CPU, it is not necessary for said memory controller to perform said data transfer instead of direct data transfer (i.e., said CPU could directly perform said data transfer if said CPU is synchronized with said image data bus; See Masayuki's prior art in Fig. 16, and paragraphs [0003]-[0006]).

Furthermore, the Examiner doubts why the host interface 31 and JPEG interface 30, and memory interface 27 are not necessary for coupling said image data bus to said CPU if said image data bus is synchronized with said CPU.
Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

*In response to the Appellant's argument with respect to* "Second, the comments in the Final Office Action regarding inherency are not understood; the principle of inherency is applicable only with respect to 35 U.S.C. § 102 rejections. Inherency and obviousness are distinct concepts. A retrospective view of inherency is not a substitute for some teaching or suggestion that supports the selection and use of the elements in the particular claimed combination. ..." in the Appeal Brief page 14, lines 4-11, the Examiner respectfully disagrees.

First of all, the Office Action has never depended on the retrospective view of inherency for any claim rejection under 35 U.S.C. §102 and/or §103 at all.

Secondly, the comment "inherency" in the argument's response of the Final Office Action is not the retrospective view of inherency because the single reference Masayuki clearly discloses that two busses are separately operating in order to prevent delay of image data bus (See Masayuki, paragraphs [0007]-[0008]). In order words, the fact of the claimed subject matters "synchronous bus" and "asynchronous bus" is clearly suggested by the single reference Masayuki in contrary to the Appellant's asserted "retrospective view of inherency" without any fact from the prior art.

At third, in contrary to the Appellant's allegation, i.e., the principle of inherency is applicable only with respect to 35 U.S.C. § 102 rejections, the inherent disclosure of a prior art may be relied upon in the rejection of claims under 35 U.S.C. §102 or §103. (See MPEP 2112

[R-3] Requirements of Rejection Based on Inherency; Burden of Proof.).

Therefore, Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

*In response to the Appellant's argument with respect to* " Further, Appellant submits that it is not inherent that image data bus 33 is (asynchronous) not synchronized with CPU 41 in Fig. 2, because evidence of inherency in a reference 'must make it clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.' Continental Can Co. USA Inc. v. Monsanto Co., 948 F.2d 1264, 1269 (Fed. Cir. 1991) (emphasis added)." in the Appeal Brief page 14, lines 4-11, the Examiner respectfully disagrees.

As is discussed in the above response, the Examiner has provided enough evidence of inherency in the reference Masayuki regarding to the claimed limitations "a synchronous bus synchronized with a processor," and "an asynchronous bus not synchronized with the processor." Moreover, the evidence described in the above response makes it clear that the missing descriptive matter, i.e., the terms related to "synchronous" and "asynchronous," is necessarily present in the thing described in Masayuki, and that it would be so recognized by persons of ordinary skill.

Thus, Appellant's argument for this point cannot be seen as persuasive.

*In response to the Appellant's argument with respect to* "Additionally, 'Inherency, however may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not probabilities or possibilities.' ... Similarly, even if the image data bus 33 could either be synchronized or not synchronized with

CPU 41, this possibility cannot be said to disclose that the image data bus is *necessarily* not synchronized when Masayuki is silent with respect to this feature." in the Appeal Brief page 14, lines 4-11, the Examiner believes that the Appellant misunderstand the claim rejection.

Basically, the Examiner agrees with the Appellant's statement in light of the case law Finnigan Corp. v. I.T.C., 51 USPQ 2d 1001, 1009-10 (Fed. Cir. 1999), i.e., Inherency may not be established by probabilities or possibilities.

However, in contrary to the Appellant's assumption, i.e., the image data bus 33 could either be synchronized or not synchronized with CPU 41 in Fig. 2 of Masayuki, said image data bus in Masayuki cannot be synchronized with said CPU because the objective of the Masayuki's invention is for preventing delay of said image data bus and can perform signal processing efficiently in each circuit (See paragraphs [0007]-[0009]), which is different from the conventional embodiment, i.e., image data bus being directly coupled to CPU 210 via CPU bus 206 (a.k.a., synchronized), shown in Fig. 16.

If said image data bus is synchronized with said CPU via said CPU bus, said image data bus not being occupied by any circuit is delayed by the CPU synchronization clock during said CPU is performing data transfer via said CPU bus.

Therefore, the Examiner has never stated that the image data bus is *necessarily* not synchronized with the CPU under the possible situations of the image data bus being synchronized or not synchronized with the CPU, and thus, the Appellant's argument on this point appears to be in error and should not be held as persuasive for patentability.

**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/CEL/

CHRISTOPHER E. LEE
PRIMARY EXAMINER

Conferees:

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

EDDIE C. LEE
SUPERVISORY PATENT EXAMINER